High Efficiency Wide Load Range Buck/Boost/Bridge Photovoltaic Microconverter

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***Abstract*— Series strings of photovoltaic modules with integrated dc-dc microconverters can harvest more energy compared to conventional string-inverter architectures if the arrays are partially shaded or the modules mismatched. This work presents a multi-mode dc-dc converter as a candidate microconverter topology for photovoltaic modules. The topology constitutes a single inductor and four switching devices and can function in either buck, boost or an intermediate bridge mode based on the load. The proposed maximum power point tracking scheme is capable of tracking the true maximum even in partially-shaded PV modules. An experimental prototype demonstrates efficiency above 95 % at 215 W over a load range of 3 A to7 A.**

I. Introduction

Grid-tied Photovoltaic (PV) installations are commonly built with arrays of PV modules series-connected to string inverters as shown in Fig. 1. An emerging system architecture that supplements the string-inverter paradigm involves dc-dc converters (referred to here as microconverters) dedicated to individual PV modules. Figure 2 illustrates a typical setup involving microconverters. Several advantages of microconverters have been postulated and demonstrated [1]-[2]. In particular, conventional systems are known to under perform if individual modules in a series string are partially shaded (due to cloud cover or shadowing), illuminated non-uniformly (due to different roof angles in residential settings), or mismatched (due to aging or manufacturing differences). Microconverters address these problems by implementing maximum power point tracking (MPPT) at the individual PV module level so that underperforming modules do not constrain the whole string / array.

Reference [1] presents a comparison of basic power-converter circuits (buck, boost, buck-boost, and Cúk) adopted as PV microconverters. Our work seeks a topology and control technique that maximizes versatility and efficiency. The chosen circuit extends the buck-boost power stage presented in [2] by introducing an intermediate bridge mode that enables continuous maximum power point tracking (MPPT). Based on load current, the digital control scheme manages a seamless transfer across switching modes on a cycle-by-cycle basis. Synchronous rectification achieves efficiency above 95%, while a high switching frequency of 250 kHz enables the use of small passive components, eliminating the need for electrolytic capacitors and guaranteeing a compact form factor.

The remainder of this paper is organized as follows. Section II describes the power stage of the proposed topology and details the different switching modes. The digital control scheme is explained in Section III. The MPPT algorithm that is robust to partial shading effects is described in Section IV. Results from an experimental prototype are described in Section V, and the conclusion is in Section VI.

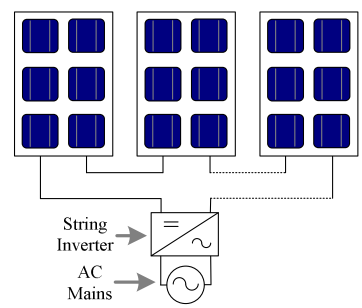

Figure 1. Conventional string-inverter architecture.

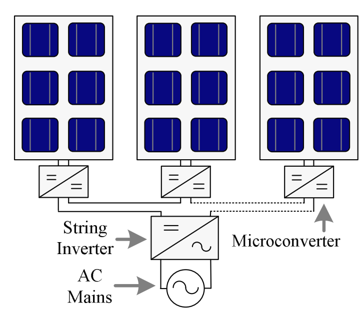

Figure 2. Emerging microconverter system architecture.

II. BUCK/BOOST/BRIDGE POWER STAGE

The power stage, illustrated in Fig. 3, comprises buck-side switches, S_1-S_2, boost-side switches, S_3-S_4, an inductor, L, and input and output capacitors, C_i and C_o, respectively. In addition, there are low-side current sensing resistors and buffer amplifiers to enable the acquisition of input and output voltage and current as well as 5V and 12V on-board house-keeping supplies powered by the PV source.

The power stage is intended to be compatible with a wide variety of PV sources and a string inverter loads. In addition, it is expected to harvest energy from partially-shaded PV sources. To accomplish these goals, the topology must operate in buck mode or boost mode.

The power stage is designed to operate at a nominal input maximum power point (MPP) of about 40 V and 5 A (I_M, V_M). The inductance is 40 µH. At the MPP, continuous current mode (CCM) buck operation is guaranteed when the input current exceeds approximately 300 mA for any buck load current. Similarly, in boost mode, CCM is guaranteed when the input current exceeds 2 A.

PWM constraints are imposed by minimum switch ON-times of 100 nsec (S_2 and S_4) and 133 nsec (S_1 and S_3) and a dead time of 150 nsec at all switch transitions. Consequently, the buck duty cycle, D_{bu} (the fraction of S_1 ON-time) cannot have a value between 0.9 and 1.0. Likewise, the boost duty cycle, D_{bo} (the fraction of S_3 ON-time) cannot exist between 0 and 0.033. The PWM method described below provides a smooth transition between the buck and boost modes as load current increases while adhering to all switching constraints.

The ideal dc gain of the converter is given by

$$G = \frac{V_o}{V_i} = \frac{I_i}{I_o} = \frac{D_{bu}}{1 - D_{bo}}. \qquad (1)$$

Buck mode switching, where $D_{bo} = 0$, is used for $0<G\leq 0.9$, where the minimum S_2 ON-time is required. Likewise, boost mode switching, where $D_{bu} = 1$, is used for $G>1.034$. The duty cycle resolution is 0.00375% (150 psec steps).

To obtain similar resolution in the buck-to-boost transition range, 0.9 < G < 1.034, bridge switching is employed. The bridge mode is divided into two regions, br_A and br_B, as shown in Fig. 4, where D_{bu} and D_{bo} are plotted as a function of converter gain. At the low-gain end of br_A, S_3 is switched on for its minimum allowable time, 133 nsec, corresponding to D_{bo} = 0.033. At the same time, D_{bu} = 0.875, which results in a gain of 0.9052. To increase the gain within the br_A region, D_{bu} is increased up to a maximum of 0.9 (again limited by S_2 minimum ON-time), corresponding to a converter gain of 0.9310. In the br_B region, D_{bo} is varied while holding D_{bu} = 0.9. The high-gain end of br_B, 1.033, is reached when a smooth transition to boost mode can be made employing the minimum S_3 ON-time. It is worth noting that, given the minimum and dead time switching constraints, this strategy achieves the minimum possible average inductor current at all values of gain and therefore minimizes the conductive losses in the inductor and the switches.

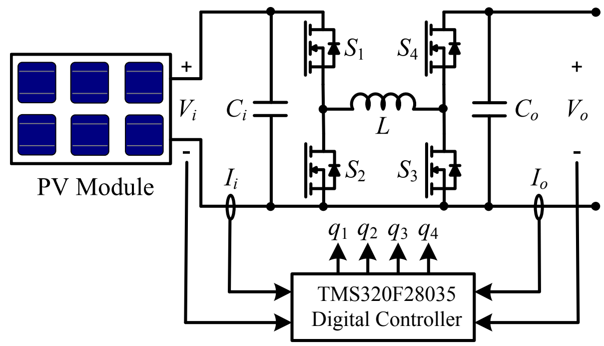

Figure 3. Microconverter power stage topology.

In bridge operation, the relative phase of S_1 and S_3 switching is chosen to minimize ripple current. The ON-time of switch S_1 (S_3) is symmetrical about the beginning (middle) of the 4 µsec switching period. Figure 5 illustrates the detail of the resulting switch waveforms of each switching mode over an 800 nsec time interval in the center of the switching period. Note that in the br_A and br-B modes, outside the brief shaded time intervals, the voltage across the inductor is approximately (or in some cases exactly) zero. Thus, the ripple current is very small, further reducing the conductive power loss in those switching modes.

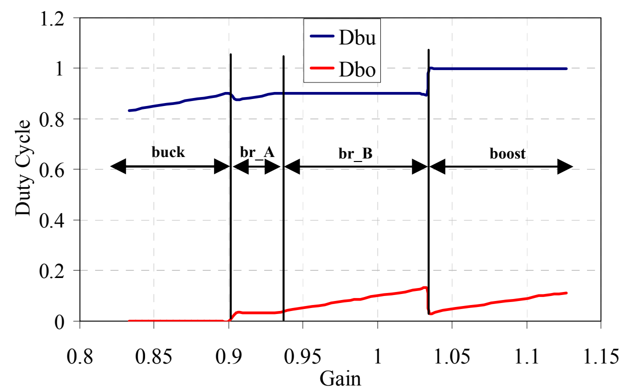

Figure 4. *Dbu* and *Dbo* in the buck-to-boost transition region.

III. TWO-LOOP DIGITAL CONTROL SCHEME

The digital two-loop control method is shown in Fig. 6. A fast inner loop controls input current, driving it to an input current reference level set by the slower outer loop that implements MPPT. The inner loop, sampling at 250 kHz, is compensated in all switching modes with a single fixed function, comprising an integrator, a real pole and a complex zero pair. The resulting fast control loop crossover frequency is approximately 1 kHz. PWM driver firmware derives both D_{bu} and D_{bo} from a single scalar output of the digital compensation filter.

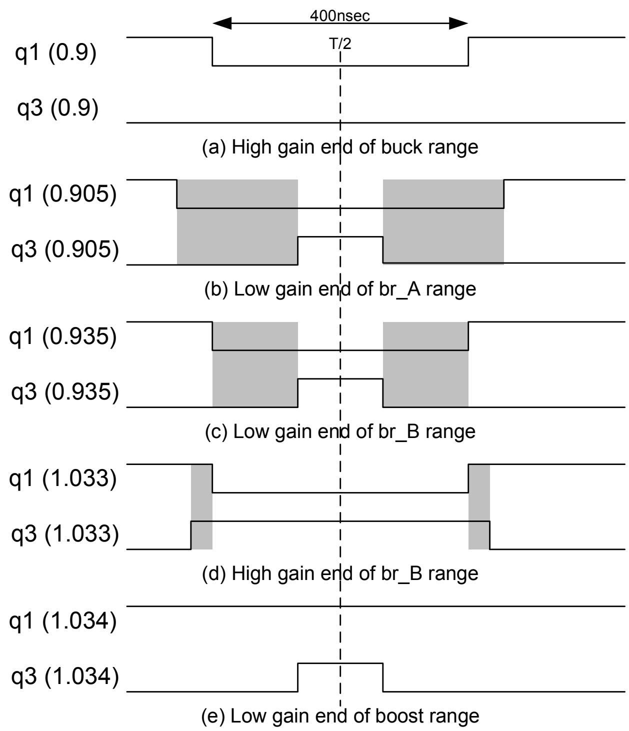

Figure 5. Detail of PWM switching in buck-to-boost transition region

Control is implemented by the TMS320F28035 microcontroller. Six channels of its 16-channel data acquisition sub-system are used. Input current and output voltage are acquired on each 4 µsec PWM cycle. Input voltage, output current, and the +5V and +12V supplies are sampled less frequently for under-voltage conditions. Three of the microcontroller's seven PWM generators are employed. One is dedicated to buck side switching, a second to boost side switching, and the third controls the phase of the analog input sampling with respect to the switch operation.

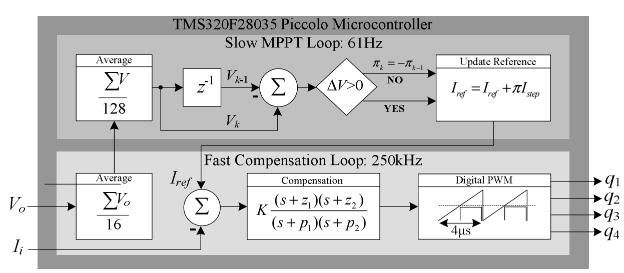

Figure 6. Block diagram of the two-loop control scheme implemented on the TMS320F28035 microcontroller.

Input current sampling and duty cycle update occur at the beginning of the switching cycle, in the center of the S_1 ON period, when switching transients produced by the S_1–S_2 commutation have subsided. This provides virtually the entire 4 µsec for control housekeeping calculations prior to updating the PWM duty at the beginning of the next carrier cycle. The resulting average control loop delay is 6 µs.

IV. Maximum Power Point Tracking Algorithm

Maximum power point tracking is implemented with a hill-climbing algorithm that is tuned to the characteristics of its associated PV module; in this case a 215 W Sanyo HIT 215N module comprising three series-connected sub-strings of 24 cells each. A bypass diode parallels each sub-string to prevent potentially damaging hot spots when partial shading conditions prevent one or more sub-strings from supporting the module's load current.

A. PV Module Characteristics

Figure 7 shows a plot of the measured output current and power versus output voltage of a module uniformly illuminated by natural sunlight. On the day when the measurements were made, the maximum module power was 202 W at 41.47 V and 4.87 A. Careful observation of the data reveals that, over 40.44 and 42.73 V, (or equivalently 4.69 and 4.96 A), the module output power remains within 99% of its peak. Notice also that the output voltage at MPP is roughly 80% of the open circuit voltage, V_{OC}.

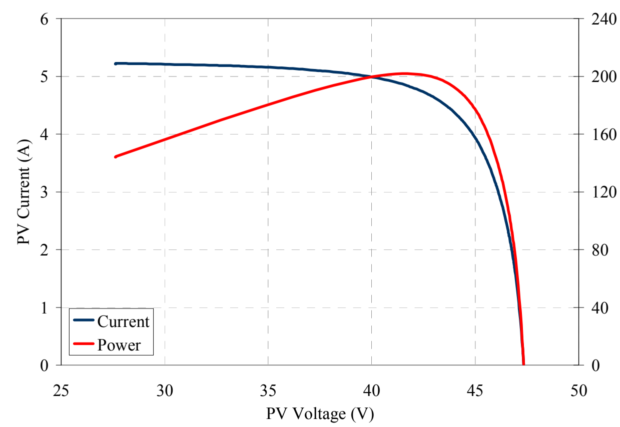

Figure 7. PV power and current versus PV voltage of uniformly lighted Sanyo HIT 215N module.

Figure 8 plots the PV power and current versus PV voltage when non-uniform shading causes one bypass diode to conduct a portion of the load current. This is manifest by the rapid drop in PV voltage when the load current exceeds about 750 mA. At higher load current, the bypass diode across the shaded sub-string conducts. As a result, the voltage across it collapses from about 15 V to about -1 V, the bypass diode forward bias voltage.

In the case exhibited in Fig. 8, the weakly illuminated sub-string supports only a maximum of 700-750 mA, and the load current corresponding to maximum power harvesting from it is in that range. Maximum power harvesting from the other two groups of PV cells requires about 1.6 A. Thus, there are two peaks in the power curve, and the MPPT algorithm must determine which is the true maximum.

Lighting conditions may cause two diodes to conduct, producing a third peak in the power curve at roughly, $0.25V_{OC}$. In general, a module with N diodes may exhibit N peaks under specific, albeit rare, lighting conditions.

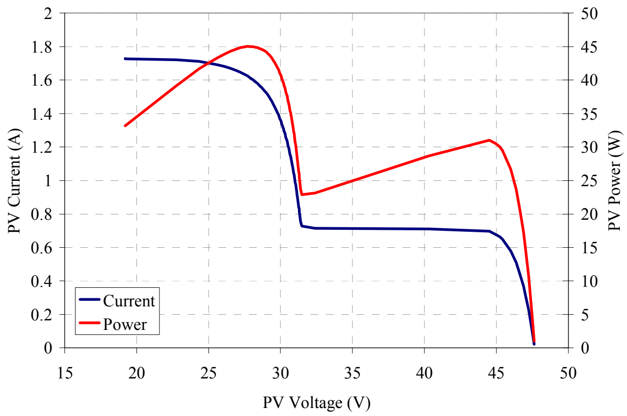

Figure 8. PV power and current versus PV voltage when one group of 24 cells is shaded more than the others.

B. MPPT Algorithm details

Maximum power point tracking is intended to harvest the maximum available power from the PV module. It is most frequently implemented by continuously running algorithms that maximize the product of the microconverter input voltage and current. We report here results obtained by maximizing the output voltage. We justify this with several assertions: First we cite reference [3], a manuscript dedicated to the idea. Second, after examining the input current and voltage of string inverters available to us, we conclude that they present a very slowly-varying current load to the microconverter. As long as the MPPT algorithm is fast with respect to the inverter input current changes, maximizing output voltage is equivalent to maximizing output power. Third, maximum output power is the goal, and using it directly in the algorithm, rather than input power, accounts for any microconverter efficiency variation. Finally, accurate current measurement is difficult. It adds noise, and power computation is a burden to algorithms that maximize power.

Based upon observations reported in Section IV A, the MPPT algorithm implemented here, begins with the assumption that there may be as many as three peaks in the power curves of the Sanyo modules located in the vicinity of $0.75V_{OC}$, $0.5V_{OC}$, and $0.25V_{OC}$. A simple hill-climbing algorithm will find and track the true maximum peak if it starts near it. This is done by initiating operation in four stages. In the first, all switching is halted, and after sufficient settling time, the open circuit voltage is sampled. In stage two, the PV output current is increased until its output voltage drops to $0.75V_{OC}$ at which time the microconverter output voltage and the PV module output current are recorded. This is repeated for $0.50V_{OC}$ and $0.25V_{OC}$ in stages three and four, respectively. Finally, operation shifts to stage 5, continuous MPPT using the perturb-and-observe algorithm, starting at the PV output current corresponding to the highest microconverter output voltage observed in stages two through four. Stage five operation persists until a change in output voltage greater than a prescribed amount (programmable) is detected, at which time the initiation sequence is repeated.

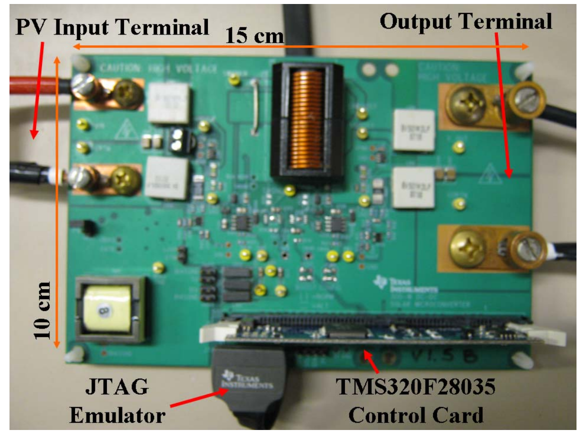

Figure 9. Microconverter experimental prototype

V. EXPERIMENTAL PROTOTYPE

A prototype of the proposed microconverter has been built and tested. The printed circuit board, shown in Fig. 9, comprises the power stage including all switches, drivers, passives, 12 V and 5 V housekeeping supplies powered by the PV source, and an edge connector for the control board that contains the TMS320F28035 microcontroller and a 3.3 V LDO. All four switches are TCPA8054 n-channel MOSFETs. Each pair, S_1- S_2 and S_3- S_4, is driven by a UCC27201 that provides both high- and low-side drivers. The high-side driver employs a bootstrapped internal supply that must be periodically refreshed, every 2 msec in this implementation. The envisioned application is internal to solar modules, and this prototype firmware is tuned for the 215 W Sanyo HIT PV modules. Relevant parameters of the experimental prototype and the PV module are listed in Table I.

TABLE I
MICROCONVERTER AND PV MODULE PARAMETERS

Symbol	Quantity	Value
L	Inductance	40 µH
C_i	Input capacitance	15.4 µF
C_o	Output capacitance	15.4 µF
f_{SW}	Switching frequency	250 kHz
V_M	MPP voltage (STC)	42.0 V
I_M	MPP current (STC)	5.13 A
P_M	Maximum power	215 W
V_{OC}	Open-circuit voltage	51.6 V
I_{SC}	Short-circuit current	5.61 A

The scope trace shown in Fig. 10 illustrates the microconverter initialization sequence described in the previous section. In this particular example, in order to display clearly each of the stages of the process, the sequence completes in about 7 seconds, but it can easily be executed an order of magnitude faster.

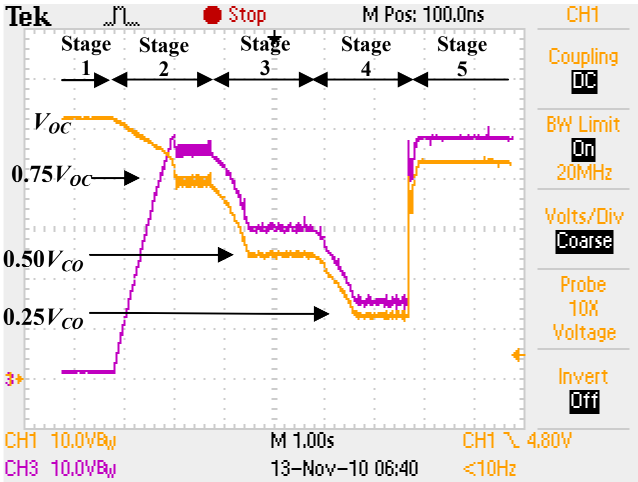

Figure 10. Scope trace of PV module (orange) and microconverter (purple) outputs during each phase of the MPPT algorithm.

The scope capture in Fig. 11 illustrates the transient behavior of PV voltage, V_i, and output voltage, V_o, due to steps in load current, I_o while continuously tracking the maximum power point. In this test, the MPP PV current is 2.5 A. At time t_1, the load is stepped from 2.75 A to 2.25 A. This causes a change in mode of operation from buck to boost mode. At time t_2, the load is stepped back up to 2.75 A, and the converter returns to buck mode. In each case, the settling time is on the order of 10 ms. The settling waveforms differ because the PV source is biased at its maximum power point and the sudden step current increase at t_2 causes a large drop in the PV voltage due to its steep decline with increasing PV current above its maximum power current.

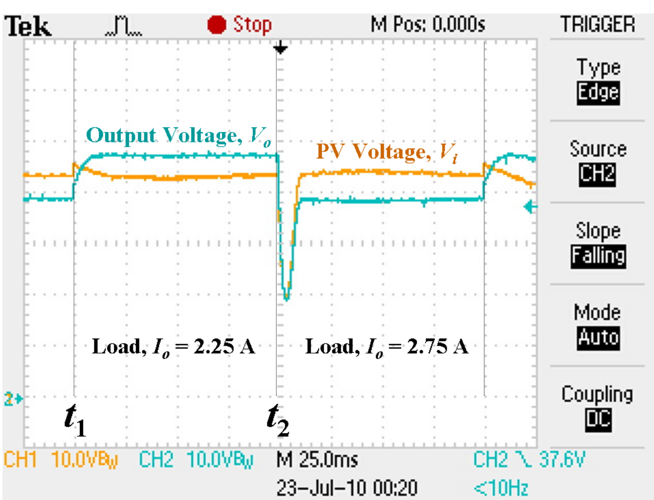

Figure 11. Transient response of micro-converter to +/-0.5 A load steps.

The total efficiency of the converter operated at MPPT for a range of load currents is plotted in Fig. 12. Total efficiency here represents the percentage of potentially harvestable electrical power. Total efficiency is diminished either by circuit losses or by MPP error.

Buck (boost) mode total efficiency approaches (exceeds) 97%, while the bridge mode is about 1% lower, due to increased switching losses. Here, the MPP is within a few tens of milliamps of the ideal. Total efficiency is limited by circuit losses: ~1% in control overhead, ~1% in conductive and ~1% in switching. The solid curve represents total efficiency when the load is directly connected to the module (S_1-S_4 ON). When directly connected, a mismatch of load current with MPP current by as little as 150 mA diminishes the total efficiency below that of the microconverter operating in bridge mode.

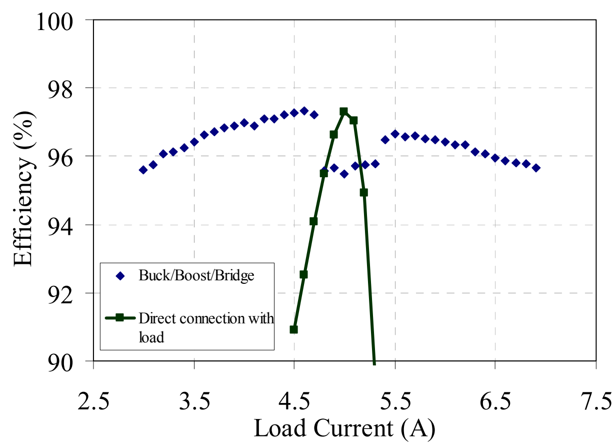

Figure 12. Measured total efficiency of the switching micro-converter (diamonds) and a direct connection (squares) versus load current.

VI. SUMMARY

A digitally-controlled multi-mode PV microconverter is proposed. Two-pole/two-zero compensation is implemented digitally and regulates the input current to a reference level determined by a hill-climbing MPPT algorithm. A seamless transition from buck to boost modes is achieved with high efficiency. The maximum power point tracking algorithm, tailored to a given PV module topology, avoids tracking errors caused by module partial shading conditions. The experimental prototype demonstrates efficiency at or above 95 % over a wide load range from 3 A to 7 A when the PV module is fully illuminated (1 sun).

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